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10/654,852	09/04/2003	Christopher S. MacLellan	EMC-03-066	5274

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,852	MACLELLAN ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/4/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-56 have been submitted for examination
- Claims 1-56 have been rejected

Claim Rejections - 35 USC § 112

1. Claims 12, 29 and 47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim12 recites:

"The method of claim 4 wherein if no errors are present in the N bits of the digital word, the second error correction code **is one** of identical to the first error correction code **and** opposite to the first error correction code".

Correction is requires

The Examiner notes the claim 12 should recite:

a. The second error correction is **either** identical to the first error correction code **or complement** to the first error correction code.

(Note: page 12, lines (4-14) in the specification)

Correction is required

b. The Second error correction is the **complement** to the first error correction in case of a data word having add parity. The applicant citation of **opposite** is indefinite, it can be complement, reverse or mirror image.

Correction is required

3. Claims 29 and 47 are rejected for the same reasons as per claim 12.

4. Claims 6, 7, 23 , 24 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 6 recites: ".....Z bits, all of which being one of all zeros **and** all ones". The phrase "**and**" renders the claim 6 indefinite. Claim 6 should recite: The Z bits, all of which being one of **either** all zeros or **all** ones Correction is required.

6. Claims 7, 23, 24 and 41 are rejected for the same reasons as per claim 6.

7. Claims 13, 30, 48 and 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 13 recites: "The method of claim 4 wherein if no errors are present in the N bits of the digital word, the digital signature comprises one of all zeros **and** all ones".

The phrase "**and**" renders the claim 13 indefinite. Claim13 should recite:

The digital signatures comprise **either** all zeros **or** all ones.

Correction is required.

9. Claims 30, 47 and 54 are rejected for the same reasons as per claim 13.

10. Claims 17, 34 and 52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 17 recites: "……error correction code is opposite the first error……."

The applicant citation of **opposite** is indefinite, it can be complement, reverse or mirror image. Claim 17 should recite:

"……error correction code is **complement** the first error……."

Correction is required.

12. Claims 34 and 52 are rejected for the same reasons as per claim 17.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams US publication no. 2004/0133836 (Hereinafter Williams)

14. In regard to claim 1, Williams teaches:

- A method for operating a data processing system comprising:
- receiving a digital word having N bits of data and M bits for error detection;

  (Note: DATA IN (DATA+ECC1) in Figure 6, in Williams)
- B. generating a first error correction code based on the N bits of data of the digital word;

  (Note: Figure 6, reference character (330A) in Williams)
- C. generating a second error correction code based on the N bits of data of the digital word;

  (Note: Figure 6, reference character (330B) in Williams)
- D. performing a first logic operation on the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code;

  (Note: Figure 6, reference character (410) in Williams)
- E. performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word;

  (Note: Figure 6, reference character (420) in Williams)
- F. comparing the generated constant signal to a predetermined constant signal, and

(Note: Figure 6, reference characters (415) and (420) in Williams)

- G. determining that an error has occurred in at least one of the N bits of data in the digital word, the M bits of the digital word, the first error correction code and the second error correction code if the generated constant signal is different from the predetermined constant signal.

(Note: Figure 6, reference character (420) in Williams)

15. In regard to claim 2, Williams teaches:

- The method of claim 1 wherein the first error correction code includes Y bits, wherein each one of the Y bits is generated by performing a third logic operation on predetermined bit sets of the digital word.

(Note: Section [0009] in Williams)

16. In regard to claim 3, Williams teaches:

- The method of claim 2 wherein at least two of the Y bits of the first error correction code are generated by performing the third logic operation on different predetermined bit sets of the digital word.

(Note: Section [0011] in Williams)

17. In regard to Claim 4, Williams teaches:

- The method of claim 3 wherein the second error correction code includes Y bits, wherein each one of the Y bits of the second error correction code is generated by performing a fourth logic operation on bits of the digital word which are not included in the predetermined bit

set of the digital word used to generate a corresponding bit of the first error correction code.

(Note: Section [0047], line (10), reference character (330B))

17. In regard to claim 5, Williams teaches:

- The method of claim 1 wherein the M bits of the digital word for error Correction are Parity bits.

(Note: Section [0009] in Williams)

19. In regard to claim 6, Williams teaches:

- The method of claim 4 wherein the predetermined constant signal comprises Z bits, all of which being one of all zeros and all ones.

(Note: Figure 6, reference character (420) the inputs to the OR gate in Williams)

20. In regard to claim 7, Williams teaches:

- The method of claim 6 wherein the generated constant signal comprises Z bits and, if no errors are present in at least one of the N bits of data in the digital word, the M bits of data in the digital word, the first error correction code and the second error correction code, all of the Z bits of the generated constant signal are one of all zeros and all ones.

(Note: Figure 6, reference characters (410) and (415) in Williams)

21. In regard to claim 8, Williams teaches:

- The method of claim 7 wherein the first logic operation is an XOR operation.

  (Note: Figure 6, reference character (330A) in Williams)

22. In regard to claim 9, Williams teaches:

- The method of claim 8 wherein the second logic operation is an XOR operation.

  (Note: Figure 6, reference character (330B) in Williams)

23. In regard to claim 10, William teaches:

- The method of claim 9 wherein the third logic operation is one of an XOR operation and an XNOR operation.

  (Note: Figure 6, reference character (410) in Williams)

24. In regard to claim 11, Williams teaches:

- The method of claim 10 wherein the fourth logic operation is one of an XOR operation and an XNOR operation.

  (Note: Figure 6, reference character (415) in Williams)

25. In regard to claim 18, Williams teaches:

- A data processing system comprising:
- an input portion for receiving a digital word having N bits of data and M bits for error detection,

  (Note: DATA IN (DATA+ECC1) in Figure 6, in Williams)

- a first error correction code generator for generating a first error correction code based on the N bits of data of the digital word;

(Note: Figure 6, reference character (330A) in Williams)

- a second error correction code generator for generating a second error correction code based on the N bits of data of the digital word;

(Note: Figure 6, reference character (330B) in Williams)

- a first logic operator for performing a first logic operation on the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code;

(Note: Figure 6, reference character (410) in Williams)

- a second logic operator for performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word, and

(Note: Figure 6, reference character (420) in Williams)

- a comparator for comparing the generated constant signal to a predetermined constant signal and generating an error signal indicating that an error has occurred in at least one of the N bits of data in the digital word, the M bits of the digital word, the first error correction code and the second error correction code if the generated constant signal is different from the predetermined constant signal.

(Note: Figure 6, reference characters (415) and (420) in Williams)

(Note: Figure 6, reference character (420) in Williams)

26. Claim 19 is rejected for the same reasons as per claim 2.

27. Claim 20 is rejected for the same reasons as per claim 3.

28. Claim 21 is rejected for the same reasons as per claim 4.

29. Claim 22 is rejected for the same reasons as per claim 5.

30. Claim 23 is rejected for the same reasons as per claim 6.

31. Claim 24 is rejected for the same reasons as per claim 7.

32. Claim 25 is rejected for the same reasons as per claim 8.

33. Claim 26 is rejected for the same reasons as per claim 9.

34. Claim 27 is rejected for the same reasons as per claim 10.

35. Claim 28 is rejected for the same reasons as per claim 11.

36. In regard to claim 35, Williams teaches:

- A method for operating a data processing system comprising:
- A. receiving a digital word having N bits of data and M bits for error detection;

  (Note: DATA IN (DATA+ECC1) in Figure 6, in Williams)
- B. generating a primary error correction code based on the N bits of data of the digital word;

  (Note: Figure 6, reference character (330A) in Williams)
- C. generating a complementary error correction code based on the N bits of data of the digital word;

  (Note: Figure 6, reference character (410) in Williams)

- D. performing a first logic operation on the primary error correction code and the complementary error correction code to generate a data signature representative of a comparison of the primary error correction code and the complementary error correction code; and
(Note: Figure 6, reference character (410) in Williams)
- E. determining whether an error has occurred in at least one of the N bits of the digital word, the M bits of the digital word, the primary error correction code and the complementary error correction code based on the value of the data signature.
(Note: Figure 6, reference characters (415) and (420) in Williams)

37. In regard to claim 36, Williams teaches:

- The method of claim 35 wherein Step E includes:
- performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word;
- comparing the generated constant signal to a predetermined constant signal', and
- determining that an error has occurred in at least one of the N bits of data in the digital word, the M bits of the digital word, the primary error correction code and the complementary error correction code if the generated constant signal is different from the predetermined constant signal.

(Note: Figure 6, reference character (420) in Williams)

38. Claim 37 is rejected for the same reasons as per claim 2.

39. Claim 38 is rejected for the same reasons as per claim 3.

40. Claim 39 is rejected for the same reasons as per claim 4.

41. Claim 40 is rejected for the same reasons as per claim 5.

42. Claim 41 is rejected for the same reasons as per claim 6.

43. Claim 42 is rejected for the same reasons as per claim 7.

44. Claim 43 is rejected for the same reasons as per claim 8.

45. Claim 44 is rejected for the same reasons as per claim 9.

46. Claim 45 is rejected for the same reasons as per claim 10.

47. Claim 46 is rejected for the same reasons as per claim 11.

48. In regard to claim 53, Williams teaches:

- The method of claim 35 further comprising:
- F. performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word; and (Note: Figure 6, reference character (420) in Williams)
- G. determining that an error has occurred in at least one of the N bits of data in the digital word, the M bits of data in the digital word, the primary error correction code and the complementary error correction code if the generated constant signal comprises zeroes and ones. (Note: Figure 6, reference character (420) in Williams)

49. Claim 54 is rejected for the same reasons as per claim 13.

50. Claim 55 is rejected for the same reasons as per claim 35.

51. Claim 56 is rejected for the same reasons as per claim 36.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

52. Claims 12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claims 1-4 above, and further in view of Chen US patent no. 6675349 (Hereinafter Chen).

53. In regard to claim 12, Williams teaches substantially all the limitations in claims 1-4.

However, Williams does not disclose:

- The method of claim 4 wherein if no errors are present in the N bits of the digital word, the second error correction code is one of identical to the first error correction code and opposite to the first error correction code.

Chen, in an analogous art, that teaches error correction coding of data blocks with parity bits, discloses constructing of error correcting codes of odd weight matrix and even weight matrix with at least SEC-DED coding capabilities. (Note: Col. 5, lines (54-60) in Chen)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Williams with the teaching of Chen to include use of true/complement ECC of data including odd/even parity bits. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to provide a mechanism in which errors can be indicated as occurring in a specific one of the parity bits or in a specific non-parity bit (that is, in data bit) or even in one of the ECC bits.

54. In regard to claim 16, Chen teaches:

- The method of claim 12 wherein if the N bits of the digital word are even, and if no errors are present in the N bits of the digital word, the

second error correction code is identical to the first error correction code.

(Note: Col. 6, lines ((8-17) in Chen)

55. In regard to claim 17, Chen teaches:

- The method of claim 12 wherein if the N bits of the digital word are odd, and if no errors are present in the N bits of the digital word, the second error correction code is opposite the first error correction code.

(Note: Col. 5, lines ((62-67) in Chen)

56. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claims 1-4 above, and further in view of Marianetti, II US patent 6757862 (Hereinafter Marianetti).

57. In regard to claim 13, Williams substantially teaches all the limitations in claims 1-4.

However, Williams does not disclose:

- The method of claim 4 wherein if no errors are present in the N bits of the digital word, the digital signature comprises one of all zeros and all ones.

Marianetti, in an analogous art, that teaches a method for generating an ECC for a sequence of data units, discloses ECC modification utilizing the parity of the N bits of the digital word. (Note: the Abstract in Marianetti)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Williams with the teaching of Marianetti to include ECC modification utilizing the parity of the N bits of the digital word. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to validate ECC whilst the data of the data bock is being retrieved.

58. In regard to claim 14, Marianetti teaches:

- The method of claim 13 wherein if the N bits of the digital word are even, and if no errors are present in the N bits of the digital word, the digital signature comprises all zeros.

  (Note: Col. 13, lines (35-27) in Marianetti)

59. In regard to claim 15, Marianetti teaches:

- The method of claim 13 wherein if the N bits of the digital word are odd, and if no errors are present in the N bits of the digital word, the digital signature comprises all ones.

  (Note: Col. 13, lines (28-45) in Marianetti)

60. Claim 29 is rejected for the same reasons as per claim 12.

61. Claim 30 is rejected for the same reasons as per claim 13.

62. Claim 31 is rejected for the same reasons as per claim 14.

63. Claim 32 is rejected for the same reasons as per claim 15.

64. Claim 33 is rejected for the same reasons as per claim 16.

65. Claim 34 is rejected for the same reasons as per claim 17.

66. Claim 47 is rejected for the same reasons as per claim 12.

67. Claim 48 is rejected for the same reasons as per claim 13.

68. Claim 49 is rejected for the same reasons as per claim 14.

69. Claim 50 is rejected for the same reasons as per claim 15.

70. Claim 51 is rejected for the same reasons as per claim 16.

71. Claim 52 is rejected for the same reasons as per claim 17.

72. Claim 53 is rejected for the same reasons as per claim 18.

Conclusion

73. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Blake et al., US patent no. 5682394 teaches fault tolerant computer memory systems and components employing dual level error correction and detection with disablement feature.
- Zook, US patent no. 6048090 teaches error correction and concurrent verification of a product code
- Sebaa, US patent no. 5925144 teaches error correction code circuit that performs built-in self test
- Poirier et al., US patent no. 6745363 teaches early error detection using ECC

- Chen et al., US patent no. 6675341 teaches extended error correction for SEC-DED codes with package error detection ability.
- Cooper US patent no. 6397357 teaches method of testing detection and correction capabilities of ECC memory controller.
- Takahashi et al. US publication no. 2003/0086306 teaches Semiconductor memory devices equipped with error correction circuit.
- Garcia et al., US patent no. 56644583 teaches soft error correction technique and system for odd weight row error correction codes
- Cargnoni et al., US publication no. 2004/0210814 teaches application of special ECC matrix for solving stuck bit faults in an ECC protected mechanism.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

2/10/06

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